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HDL Designer Series™ Release Notes

Release v2018.1

Note - Viewing PDF files within a web browser causes some links not to function (see MG595892).
Use HTML for full navigation.

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Chapter 1
Configuration and Compatibility

Configuration Requirements

This release of HDL Designer Series™ (HDS) tool is 2018.1.

Platform Availability

HDL Designer Series is supported on the following platforms:

- Windows 10 (64 bit)
- Windows 7 (64 bit)
- Red Hat Enterprise Linux 7 (64 bit)
- Red Hat Enterprise Linux 6 (64 bit)

Please note that DesignChecker executable and engines, Register Assistant, and SystemVerilog-VHDL Assistant are now true 64-bit applications. HDL Designer executable, *hdldesigner(.exe)*, is still a 32-bit application.

System Requirements

The minimum system requirements are as follows:

Linux

Approximately 1.2 GByte available hard-disk space
At least 2 GByte RAM and 8MByte VRAM
High color (16-bit or 65536 colors) at minimum resolution 1280x1024

Note

Please refer to “Linux Configuration” on page 7 for information on mandatory fonts and 32-bit system libraries.

Windows

Approximately 1.2 GByte available disk space
At least 2 GByte RAM and 8MByte VRAM
High color (16-bit or 65536 colors) at minimum resolution 1280x1024

Platform Configuration

There are platform configuration notes to take into consideration whether you are using HDL Designer Series on Windows® or Linux®[1].

Windows Configuration

HDL Designer Series is supported on Windows 7 and Windows 10.

TCP/IP Configuration

TCP/IP networking must be enabled in the Windows control panel if you want to use downstream tools for compilation and simulation.

Display Configuration

You should set your monitor display properties to use the maximum number of colors (16-bit high color or better on Windows) small fonts and maximum desktop area.

Refer to the “System Requirements” on page 5 for the minimum usable configuration.

Using Extended Pathnames

The HDL Designer Series products support extended pathnames. However, if you want to use an external text editor or downstream tool that does not support spaces in absolute pathnames, you should ensure that your design data is stored using pathnames without any spaces or non-standard characters.

Log Window Timeout

Interprocess communication protocol is used to communicate with downstream tools. This protocol can sometimes be unreliable on a Windows PC and it may not be possible to re-invoke the downstream simulator from within HDL Designer.

If this problem occurs, you should set the HDS_LOG_TIMEOUT environment variable to a low value (such as 5 seconds) to ensure that the log displayer process stops after exiting the simulator and does not prevent the simulator from being re-invoked.

Note that if you specify a very short timeout, some of the output from the downstream tool may be lost. If you specify a very long timeout, the log displayer process may take a long time to end.

1. Linux® is a registered trademark of Linus Torvalds in the U.S. and other countries.

Using Anti-virus Software

If you experience problems running downstream tools on a Windows PC, this may be caused by the anti-virus software treating the communications pipe as a file.

This results in the pipe being opened in a “deny all” mode which prevents client software from reading or writing to the pipe. This problem can be avoided if the anti-virus software is configured to scan program files only. Alternatively, contact the vendor of your anti-virus software for advice on configuring the software so that it does not prevent communications between client applications.

Note also that some anti-virus programs can change the case of a filename or automatically delete files with certain file extensions. For example, problems may occur if the virus checker has been configured to quarantine files with extensions used by HDL Designer resource files such as visual resource files (*.vrf*) files.

Linux Configuration

HDL Designer Series is supported on Red Hat Enterprise Linux 6 and 7.

Verifying Fonts

If you are using Red Hat Enterprise Linux 6 or 7, you can encounter errors on the invocation of HDL Designer Series if some required fonts are not found.

You need to make sure that the following fonts are installed:

- xorg-x11-fonts-ISO8859-1-75dpi
- xorg-x11-fonts-ISO8859-1-100dpi

This can be done by following these steps:

1. Determine the font path being referenced using the command:

   ```
   xset -q
   ```

   For example, the path can be */usr/share/X11/fonts/misc*.

2. If you do not find the 75dpi and 100dpi Helvetica fonts on the path, add them using the following commands:

   ```
   xset +fp /usr/share/X11/fonts/75dpi
   xset +fp /usr/share/X11/fonts/100dpi
   ```

3. Run the following command to rebuild the fonts cache:

   ```
   xset fp rehash
   ```

4. Check the font path again using the following command:

```
xset -q
```

The new font paths will now be as follows:

/usr/share/X11/fonts/100dpi

/usr/share/X11/fonts/75dpi

/usr/share/X11/fonts/misc

5. Verify that the Helvetica fonts are available as follows:

```
/usr/bin/xlsfonts | grep adobe-helvetica
```

6. Verify that the Courier fonts are available as follows:

```
/usr/bin/xlsfonts | grep courier
```

Note

If the 75dpi and 100dpi directories are missing, ensure that the fonts installed are of type ISO. For example: *yum install xorg-x11-fonts-ISO8859-1-75dpi.noarch*

Required Libraries

You need to install certain 32-bit packages if you are running HDL Designer Series on a 64-bit Linux system, otherwise you may receive errors related to missing libraries.

The following packages are required:

1. gtk2.i686
2. gtk2-engines.i686
3. libXtst.i686
4. libXt.i686
5. libstdc++.i686
6. PackageKit-gtk-module.i686
7. libcanberra-gtk2.i686
8. xulrunner.i686 (1.9.2)
9. webkitgtk.i686 (1.2.x and newer)
10. glibc.i686
11. zlib.i686
12. libgcc.i686
13. libX11.i686

14. libstdc++.x86_64
15. compat-libstdc++.x86_64

You can use the *yum* command to install these libraries as follows:

```
yum install gtk2.i686
yum install gtk2-engines.i686
yum install libXtst.i686
yum install libXt.i686
yum install libstdc++.i686
yum install PackageKit-gtk-module.i686
yum install libcanberra-gtk2.i686
yum install xulrunner.i686
yum install webkitgtk.i686
yum install glibc.i686
yum install zlib.i686
yum install libgcc.i686
yum install libX11.i686
yum install libstdc++.x86_64
yum install compat-libstdc++-33.x86_64
```

Note

If you are using QAS (Quest Authentication Services), you should install the 32-bit version of libns-vas4.so. Similarly, if you are using LDAP protocol (Lightweight Directory Access Protocol), you should install the 32-bit version of libnss_sss.so.

Required PDF Plug-in for System Verilog-VHDL Assistant

On Linux, to open PDF documents from **Help > Help and Manuals**, you need to download a PDF reader plug-in for the web browser.

New Features in 2018.1

This release includes the following new features and enhancements:

- HDL Designer:
  - Graphical support for the following VHDL 2008 constructs:
    - Extensions to generate (elsif, else, case)
    - Context design units
  - Vendor/Flow updates:
    - Supporting Intel® Quartus® Prime flow
    - Supporting Xilinx® Vivado® 2018.1

    - Supporting Questa® 10.7x
- SystemVerilog-VHDL Assistant:
    - Supporting extending parameterized classes
    - Supporting static visualization of UVMF parameterized classes
    - Improving performance
    - Upgrading to Eclipse Luna 4.4.2 and CDT 8.6.0
- DesignChecker:
    - Capacity improvement:
        - Upgrading to native full DesignChecker 64-Bit application
    - Enhancing DO-254 support:
        - Supporting Combined Report (of other selected DesignChecker reports)
        - Enhancing Summary Report as follows:
            a. Adding timestamp information
            b. Adding Ruleset/Policy paths
            c. Adding Ruleset/Policy save status
    - Improving independent batch flow:
        - Enhancing the ability to set default file dialects
        - Supporting exclusions after loading batch results
    - Supporting new VHDL 2008 constructs:
        - Extensions to generate (elsif, else, case)
        - Context design units
    - Enhancing the following base rules:
        - Asynchronous Reset Release
        - File Header
        - Input Synchronizer
        - Matching Range
    - Upgrading synthesis engine:
        - Recent language support
        - Improving quality and stability

- Register Assistant:
  - Upgrading to native 64-bit application
  - Supporting IP-XACT IEEE 1685-2009
  - Upgrading to Eclipse Luna 4.4.2
- Miscellaneous fixed defects and enhancements

Licensing SystemVerilog-VHDL Assistant

SystemVerilog-VHDL Assistant functionality is available to all users of HDL Designer Series using the composite license feature hdldesigner_c. No additional licenses are required as the new feature (svassist) is included in the new pkginfo.mgc file in 2013.1.

Installation and Licensing

HDL Designer Series provides two installers: HDL Designer and HDL Text. HDL Designer allows you to install Design Manager, SystemVerilog-VHDL Assistant, DesignPad, DesignChecker, and Register Assistant. HDL Text allows you to install SystemVerilog-VHDL Assistant and DesignChecker only.

Note

HDL Author is no longer available in the installer. If you are using HDL Author, you need to do the following in order to be able to invoke HDL Designer in Author mode:
• For Windows users, create a new shortcut with *"target": <HDS_HOME>\bin\hdldesigner.exe –authorpro.*
• For Linux users, copy *hdl_author* script from your previous HDL Author tree to the same location in the new tree.

Licensing is implemented using the PCLS or MGLS versions of the Macrovision FLEXlm license manager which are normally used for Mentor Graphics Corporation (MGC) products.

All required files to license the HDL Designer Series products are included in the installation and you do not need to explicitly install licensing unless you want to setup a separate license server.

The licensing systems all support floating licenses on a remote server and node-locked licenses indexed to a UNIX workstation hostid or to a hardware security key (dongle).

The HDL Designer Series products are compatible with existing license server installations based on FlexNet 11.14.1.3. For more information about FLEXlm including the latest version of the *License Administration Guide*, check the **Release Information** scope in the HDL Designer

Series InfoHub. The vendor daemons and lmgrd that are shipped with this release will be FlexNet version 11.14.1.3.

For floating licenses, it will be necessary to verify that the vendor daemon (i.e., mgcld) and the license server (i.e., lmgrd) have FlexNet versions equal to or greater than 11.14.1.3. If the current FlexNet version of your vendor daemon and lmgrd is less than 11.14.1.3 then it will be necessary to stop your license server and restart it using the vendor daemon and lmgrd contained in this release.

If you use node-locked licenses, you do not need to do anything. This release will update the licensing to MSL v2017_1 with MGLS v9-17_10-2-4 (v2017_1_patch2) and PCLS v9-17_10-3-0 (v2017_1_patch1).

PCLS has a new version format to better track with the associated MGLS version.

In summary, this release uses the following license versions:

- FlexNet 11.14.1.3
- MSL v2017_1
- MGLS v9-17_10-2-4 (v2017_1_patch2)
- PCLS v9-17_10-3-0 (v2017_1_patch1)

License File Location

The default license file location on a UNIX or Linux workstation is:
<install directory>/license/license.dat

The default license file location on a Windows PC is:
C:\flexlm\license.dat

You can use the MGLS_LICENSE_FILE or LM_LICENSE_FILE environment variable to specify an alternative location for the license file. Both variables are recognized by MGC licensing. However, the MGLS_LICENSE_FILE variable takes precedence if both variables are set.

Thus, LM_LICENSE_FILE can be set for applications that use standard FLEXlm licensing, while the location specified by MGLS_LICENSE_FILE is used for Mentor Graphics applications.

On windows, these variables are set in the registry when you install licensing. The precedence is:
MGLS_LICENSE_FILE set in the environment
MGLS_LICENSE_FILE set in the registry

LM_LICENSE_FILE set in the environment
LM_LICENSE_FILE set in the registry

These settings are search paths and can be set to multiple locations by entering multiple pathnames or port specifications (separated by a colon on UNIX or by a semi-colon on Windows). For example:

1700@mylichost:/usr/opt/license.dat
1700@mylichost;C:\license.dat;C:\hds\license.dat

You can check the variable and registry settings on Windows by using the **PCLS_OK** utility which can be accessed from the **Licensing** cascade for **HDL Designer Series** in the **Programs** section of your Windows **Start** menu.

Note

The PCLS_OK utility has been relocated from *HDS<release_number>\bin* directory to a separate Mentor Licensing Program directory found at *C:\MentorGraphics\Licensing*. This can be uninstalled separately from the tool.

Tip: To install the PCLS separately, you will have to navigate to the setup files at *HDS<release_number>\license\pcls_setup.exe*.

Using a Dongle on a Windows PC

A hardware security key (dongle) is not required if you are using an evaluation license or have chosen to use a remote license server. A key is required when you install licensing on the local PC (or on a PC used as a license server).

The dongle is a generic device connected to the USB and can also be used for other products although a valid license key which matches the unique identifier is required for each product.

Tip: To install the Dongle Drivers separately, you will have to navigate to the setup files at *HDS<release_number>\license\dongle_setup.exe*.

The driver can be loaded during installation or an existing driver can be checked using the **LMTOOLS** utility which can be accessed from the **Licensing** cascade for **HDL Designer Series** in the **Programs** section of your Windows **Start** menu.

Note

The **LMTOOLS** utility has been relocated from *HDS<release_number>\bin* directory to a separate Mentor Licensing Program directory found at *C:\MentorGraphics\Licensing*. This can be uninstalled separately from the tool.

Select the **System Settings** tab of the LMTOOLS dialog box. If you have the correct driver loaded, the dongle serial number should be displayed in the FLEXID field. If the displayed number does not match the serial number on your dongle, re-install the licensing system to load the correct driver.

License Maintenance Date

Existing licenses will enable this version of HDL Designer provided that the release date of the software is less than or equal to the exact access date. For example, 2007.030 in the following example:

INCREMENT hdldesignerpro mgcld 2007.030 19-mar-2007 1 ED3090278DDE24D5BF09 VENDOR_STRING=683AB64D

The version number is also commonly referred to as the license maintenance date or the exact access date. If your license incorrectly shows an expired maintenance date, please contact your local sales office.

You can examine the current license information using the FLEXlm license manager on Windows or you can use the *lmutil lmstat -A* or *lmstat -A* commands in a shell on any platform to report the licensing information in the current license file specified by the LM_LICENSE_FILE environment variable. For example:

```
"hdldesignerpro" v2007.010, vendor mgcld
```

Licensing in a UNIX MGC Environment

If you want to use an existing MGLS installation to run a HDL Designer product on UNIX, copy the contents of the *mgc.pkginfo* file from *<install_dir>/bin* into the existing file *$MGC_HOME/pkgs/mgls_rgy/lib/mgc.pkginfo* and restart the server.

MGLS licensing works in the same way as other MGC tools and if MGC_HOME is set, MGLS_HOME defaults to *$MGC_HOME/pkgs/mgls/* so need not be set explicitly.

The *mgc.pkginfo* file can be accessed from *$MGLS_HOME/lib/* or *$MGC_HOME/lib/* (which are both links to *$MGC_HOME/pkgs/mgls_rgy/lib/*).

The *mgc.pkginfo* file is required ONLY for use by the client tool that wishes to use a licence (in this case HDL Designer). It is not required by the server itself.

The following set of environment variables are recommended for using HDL Designer in an existing MGC environment:

MGLS_HOME unset
MGC_HOME set to the existing MGC tree

MGLS_LICENSE_FILE set as for your other MGC applications
LM_LICENSE_FILE unset unless required for other FLEX applications.

Refer to the *HDL Designer Series User Manual* for a full list of environment variables.

Detailed information about the Mentor Graphics Licensing System (MGLS) is given in the *Mentor Standard Licensing Manual* which is available in the installed PDF library at: *$MGC_HOME/shared/pdfdocs*. This directory also includes a copy of the FlexNet *License Administration Guide*.

New Licensing Manual

This release includes a new, rewritten *Mentor Standard Licensing Manual* that replaces the previous *Licensing Mentor Graphics Software* manual. The new manual provides streamlined, reorganized, and updated instructions and information for system administrators to use in administering Mentor Graphics software licenses. To access the new manual, choose **Help** > **Help and Manuals** to open the InfoHub, and then open the Release Information scope.

External Tool Support

The HDL Designer Series tool interfaces have been tested with certain external tool versions. Some tools may not be available on all platforms.

Downstream Tools

Tool	Version
Mentor Graphics® Model*Sim*®	10.5x, 10.6x[1] & 10.7x
Mentor Graphics® Questa®	10.5x, 10.6x[1] & 10.7x
Mentor Graphics® LeonardoSpectrum™	2016a to 2017a
Mentor Graphics® Precision®	2016.2 to 2017.2
Cadence® Incisive®	10.2 to 11.10
Synopsys® VCS®/VCSi™	2010.06 to 2011.03
Synopsys® Design Compiler®	2002.05
Synopsys® Synplify®	2016.09 to 2017.09
Intel®[2] MegaWizard™	Quartus® II 13.0 to 14.0
Intel® Quartus® Synthesis	Quartus® II 14.1 to 15.0
Intel® Quartus® SOPC Builder[3]	Quartus® II 13.0 to 14.0
Intel® Quartus® Prime	16.x to 17.x
Xilinx® CORE Generator™	ISE® 13.1 to 14.7
Xilinx® Platform Studio	ISE® 13.1 to 14.7
Xilinx® XST Synthesis	ISE® 13.1 to 14.7
Xilinx® Vivado®	2017.1 to 2018.1
Actel[4]	10.0 to 11.8
Lattice	8.1 to 8.2
Mentor Graphics® I/O Designer™	8.0

1. ModelSim/Questa 10.6 is not supported.
2. Altera® tools have been acquired by Intel®.
3. It should be noted that in Intel® Quartus®II flow, Qsys is not yet supported.
4. Only Actel Designer from Microsemi's (Actel) Libero® SOC software suite is supported.

Version Management

Tool	Version
GNU RCS (Revision Control System)	5.7
GNU CVS (Concurrent Versions System)	1.11.1p1
IBM® Rational® ClearCase®	7.0.1
ClioSoft® SOS	3.03
Microsoft® or Mainsoft® Visual SourceSafe™	6.0
Subversion®	1.6x to 1.9.3

Further Information

For the latest information about the HDL Designer Series including other related products, press releases, brochures, datasheets, presentations, multimedia demonstrations and software downloads, see the web site at:

`http://www.mentor.com/products/fpga/hdl_design/hdl_designer_series/`

For information about the DesignChecker changes in this release, you can refer to the *DesignChecker Release Notes*.

For information about the Register Assistant changes in this release, you can refer to the *Register Assistant Release Notes*.

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`https://support.mentor.com/register`

Chapter 2
Known Problems and Workarounds

This chapter lists known problems and limitations at the time of release.

- In the Allowed Types rule in DesignChecker, regarding user-entered values, if you manually enter a type name which already exists within one of the package options in the parameter list, the entry will be regarded as a duplicate and will not be retained when you close the tool.

  Workaround: To check specific types from within one of the listed packages, please prefix the type with the appropriate package name. For example, to check for type “real”, enter “std.real”. Similarly for “time”, “string” or “integer” enter “std.time”, “std.string” or “std.integer”.

- On generating VHDL for a block diagram that has been created while having the option “Convert to Graphics” set, component declarations may not be generated.

  Workaround: In VHDL, there are basically two styles of instantiations for design units: component instantiations and entity instantiations.

  Component instantiations require that a component declaration be present prior to the component instantiation. On the other hand, entity instantiations require that the entity be visible at some point before the entity is instantiated, but a component declaration is not required. HDL Designer always creates component instantiations in the VHDL generated for a block diagram or IBD. In addition, by default, it also creates component declarations in the generated code. HDL Designer currently does not give the option to generate entity instantiations.

  If you wish to supply your own component declarations in a package, HDL Designer allows you to control whether or not component declarations are created. This is affected by three factors:

  i. The “Create component declarations” option under the pulldown menu **Options>VHDL>Style**.

     This option only affects the VHDL generated for new block diagrams that you draw manually.

  ii. The “Create component declarations” option under the HDL pulldown menu in an existing block diagram.

     This option toggles whether or not component declarations will be generated for this particular diagram.

iii. The presence of component declarations in existing source code that you convert to a block diagram through the “Convert to Graphics” option.

Hence, the setting (i) determines the initial setting (ii) when you manually create a new block diagram.

After a block diagram has been created, the setting (ii) allows you to change how the VHDL is generated for that diagram.

Finally, if you use the “Convert to Graphics” option to convert existing structural code into a block diagram, the presence or absence of component declarations in the source code determines the initial setting (ii) in the block diagram that is created. Regardless of whether you create a block diagram by drawing it manually or by using the “Convert to Graphics” option, you can use the setting (ii), under the HDL pulldown menu in the diagram, to control whether component declarations are created in the generated VHDL for that diagram.

It should be noted that the above information applies to both block diagrams and IBDs.

- It is not recommended to install HDL Designer Series in a long path as this may lead to errors. The overall number of characters in the installation path is recommended to be a maximum of 80 characters. This applies to Windows only.
- If you are using Xilinx Vivado 2016.1 with the “Non-Project” mode and “Compile Simulation Libraries” option selected, then it is not recommended to compile an HDS project through the FPGA Technology Setup dialog box with “Xilinx-Vivado” set, as this raises an error.

  Workaround: Invoke the Xilinx Vivado plug-in from the Tasks browser directly, instead of invoking it through the FPGA Technology Setup task.

The following known problems can be encountered when using SystemVerilog-VHDL Assistant:

- The “Import from Questa” feature in SystemVerilog-VHDL Assistant can be used to import a design which has been previously compiled and simulated using Questa. This mechanism also imports the same Questa settings that were used in the compilation and simulation of the design including the default library search path.

  Questa 10.3 contains a new “infact” library in the default library path within the *modelsim.ini* file.

  SystemVerilog-VHDL Assistant, therefore, automatically adds the “infact” library to the “Linked Libraries” setting in the Edit Build Library dialog box, which causes the simulation to fail on Windows if there is no C compiler configured with the following message:

  ```
  Can’t locate a C/C++ compiler for ‘DPI Export Compilation’.
  ```

Workaround: Workarounds for this issue are as follows:

- If the “infact” library is not required, remove the “infact” entry from the Linked Libraries field in the Edit Build Library dialog box.
- If the “infact” library is required, make sure you have a C compiler correctly configured for use with Questa.

- HDL Designer installation paths should not contain special characters like ( ) \ / : * < > | to ensure successful operation of the SV Assistant build manager.
- On Windows, a Verilog include using a relative path can be very slow to resolve.

  Workaround: When using Verilog includes on Windows, type the full path.
- On Windows, Verilog files with include statements which start with “/” (for example */inc_dir/my_include.svh*) may take a significant time to analyze.
- In order to extract or visualize UVM/OVM objects, the UVM/OVM library source must be added to your project.
- Visualizations can only be cross-referenced during the session in which they are created. Saved visualizations are purely pictures and have no link to original code.
- Some UVM/OVM code components may not appear in the visualized testbench view when their parent classes are not referenced in a package that imports UVM/OVM.

  Workaround: Add the problematic classes to a package that imports UVM/OVM.
- If you try to add a path to any location preference on Windows using the Linux format (for example *\net\egcfs4\vol*), SystemVerilog-VHDL Assistant resolves this path (understands it as a relative path) and adds the installation drive before it.
- The SystemVerilog-VHDL Assistant “Search” operation will search within files located under the project’s directory even if they are not part of the SystemVerilog-VHDL Assistant project. Consequently, the “Open Resource” dialog box (Alt+Shift+R) displays files that are not part of the SystemVerilog-VHDL Assistant project, just because they are under the project’s directory.
- When compiling/simulating test benches, SystemVerilog-VHDL Assistant automatically detects whether the Questa used is 32-bit or 64-bit. Sometimes, SystemVerilog-VHDL Assistant does not detect that the Questa used is 64-bit.

  Workaround: Set the environment variable ‘x86_64’ to any positive value.
- Simulating UVM designs generally requires using the *uvm_dpi* shared library; when running Questa vsim, it automatically passes the right dpi options to Questa. In some rare cases, SystemVerilog-VHDL Assistant does not correctly identify the *uvm_dpi* library location.

Workaround: You can edit the command template of Questa vsim from the Project Settings to append to it the missing options "*-sv_root <Questa_uvm_dpi_library directory> -sv_lib uvm_dpi*".

- When you using the precompiled version of OVM 2.1.2 that is shipped with Questa, dynamic visualization of your simulated design might not work if your test bench has OVM components that are not registered with a factory.

  Workaround: Adding the factory registration will solve the issue. Alternatively, you can choose to compile the OVM source from within SystemVerilog-VHDL Assistant. However, in this case, you will be prompted to perform some extra steps to successfully visualize your simulated design. Detailed steps will be displayed in the Console tab when you issue the dynamic visualization command. You may also refer to the "Dynamically Visualizing UVM/OVM Testbenches" topic under the "Understanding UVM/OVM Designs" section in the *SystemVerilog-VHDL Assistant Reference Manual* which can be opened by selecting **Help> SystemVerilog-VHDL Assistant> SystemVerilog-VHDL Assistant Reference Manual**.

Broken Links in PDF Documentation - (MG595892)

Due to enhanced security restrictions with web browser PDF plug-ins, some links do not function. Links in HTML documentation are fully functional.

Clicking a link within a PDF viewed in a web browser may result in no action, or it may load the title page of the current PDF manual (instead of the intended target in the PDF manual). The unresolved link behavior occurs in all web browsers on Windows® and Linux®[1] platforms. Because of this behavior, the navigational experience of PDF manuals is compromised. PDF is ideal for printing because of its page-oriented layout.

Use the HTML manuals to search for topics, navigate between topics, and click links to examples, videos, reference material, and other related technical content.

For information about Adobe's discontinued support of Adobe Reader on Linux platforms and your available options, refer to Knowledge Article MG596568 on Support Center.

1. Linux® is a registered trademark of Linus Torvalds in the U.S. and other countries.

Chapter 3
Corrected Problems

This document lists fixed defect reports in software versions 2018.1 and earlier of the HDL Designer Series tools.

For information about new features, see *Whats New in the HDL Designer Series*.

Note

Fixed defects prefixed with *HDS-nnnn* are issues reported internally.

Software Version 2018.1

The following issues and enhancement requests have been addressed in the 2018.1 release:

HDL Designer Series

The following issues and enhancement requests have been addressed in HDL Designer Series 2018.1 release:

- **DR 1193054**

  Description: Request to support VHDL 2008 extensions to generate statement (elsif, else, and case).

- **DR 1273062**

  Description: Request to fix an issue in which Block Diagram components with bitmap graphics cannot be used to navigate down the hierarchy in HTML format.

- **DR 1298253**

  Description: Request to fix an issue in which the Xilinx Vivado flow fails to import in “Point Mode” when there is a combination of Block Diagrams and IP catalog components.

- **DR 1303860**

  Description: Request to fix a crash that occurs while importing a VHDL file with generic subprograms.

- **DR 1304082**

  Description: Request to enhance a misleading error message raised when an include file is not found.

- **DR 1305934**

Description: Request to fix an issue in which the Xilinx Vivado flow fails when using precompiled libraries.

DesignChecker

The following issues and enhancement requests have been addressed in DesignChecker 2018.1 release:

- **DR 459695**

  Description: Request to fix the ability to print out a full message when running HDL Designer Series with DesignChecker in batch mode.

- **DR 1223252**

  Description: Request to add a new parameter to the Matching Range base rule that allows ignoring integers and natural types from checks.

- **DR 1241797**

  Description: Request to fix the calculation of quality scoring, which is incorrect in the first analysis if there is a disabled base rule.

- **DR 1279362**

  Description: Request to enhance the support of externally synchronized signals in the Input Synchronizer base rule.

- **DR 1279666**

  Description: Request to enhance the File Header base rule to add a parameter value that differentiates between the top-level file and other files.

- **DR 1279671**

  Description: Request to raise a confirmation message before running analysis when there are unsaved changes in policy/rulesets, and to add information indicating if the policy/ruleset is saved or modified.

- **DR 1279674**

  Description: Request to show more information in DesignChecker reports such as the policy path, policy timestamp, analysis timestamp and DesignChecker version.

- **DR 1289827**

  Description: Request to enhance the Allowed Types base rule to fully support generic types as defined in VHDL 2008.

- **DR 1292570**

  Description: Request to fix the ability to show/hide exclusions with the loadResults API command.

- **DR 1298492**

  Description: Request to enhance the Asynchronous Reset Release base rule to support a new synchronizer circuit.

- **DR 1299293**

  Description: Request to improve the documentation of the getFiles DesignChecker API command.

- **DR 1299486**

  Description: Request to enhance the Exclusions tab to indicate if an exclusion is valid or invalid.

- **DR 1299487**

  Description: Request to show additional information in the Exclusions tab and Exclusions report.

- **DR 1299824**

  Description: Request to fix a crash that occurs in DesignChecker synthesis engine due to memory allocation errors.

- **DR 1302052**

  Description: Request the ability to add/remove exclusions on results loaded using the loadResults API command and to save these exclusions in the global constraints file for future analysis.

- **DR 1302152**

  Description: Request to fix an unnecessary warning message raised on using the setBlackBox API command on all files in a library.

- **DR 1303036**

  Description: Request to fix inconsistent behavior by the Asynchronous Reset Release base rule.

- **DR 1303037**

  Description: Request to enhance the Input Synchronizer base rule to distinguish between input ports that are not synchronized and those not sufficiently synchronized.

- **DR 1303365**

  Description: Request to fix the ability to set the project default dialect in the DesignChecker independent batch mode.

- **DR 1303643**

  Description: Request to highlight exclusions as invalid if a design unit or file is not part of the analyzed design.

- **DR 1304406**

  Description: Request to change the label “Description” to “Justification” in the Add Code/Rule Exclusions dialog box and in the Code/Rule Exclusions pane of the Exclusions tab.

- **DR 1306111**

Description: Request to fix an issue in which the VHDL Statement Order base rule does not report violations for the “if generate” statement order.

- **DR 1308092**

  Description: Request to fix an issue in which the DesignChecker constraints file is overwritten when running DesignChecker in independent batch mode, even when exclusions are not changed.

- **DR 1308454**

  Description: Request to fix a deep analysis failure that occurs on analyzing a design in DesignChecker independent batch mode.

- **DR 1311021**

  Description: Request to fix an issue in which DesignChecker in batch mode does not create *.tbc* files or reports, if no violations are raised or if all violations have been excluded.

- **DR 1312087**

  Description: Request to fix a DesignChecker hang caused by a cyclic package reference.

- **DR 1312856**

  Description: Request to enhance the Statement Labels base rule to handle all concurrent statements inside VHDL blocks and generate statements.

- **DR 1313406**

  Description: Request to automate the detection of vendor libraries and to set black box/Don’t Touch during import from Questa.

- **DR 1314921**

  Description: Request to fix an issue in which valid syntax for a local parameter causes a syntax error.

- **DR 1314933**

  Description: Request to fix an issue in which valid syntax for a package import causes a syntax error.

- **DR 1317002**

  Description: Request to restore missing items in the Design Quality Options dialog box on Linux.

SystemVerilog-VHDL Assistant

The following issues and enhancement requests have been addressed in SystemVerilog-VHDL Assistant 2018.1 release:

- **DR 1076298**

  Description: Request to fix the “Extend this class” operation to take parameters into account.

- **DR 1302957**

Description: Request to fix an error raised on deleting a file from the File Explorer Browser.

- **DR 1304177**
  Description: Request to enhance the text in the Build Management page of the Preferences dialog box.
- **DR 1304178**
  Description: Request to have a default path for the generated Makefile in the Build Management page of the Preferences dialog box.
- **DR 1316450**
  Description: Request to fix a crash that occurs after running DesignChecker on a specific test case.

Register Assistant

The following issues and enhancement requests have been addressed in Register Assistant 5.0 release:

- **DR 1236358**
  Description: Request to support recent versions of IP-XACT.
- **DR 1313313**
  Description: Request to fix a Java heap error raised when running Register Assistant.

Software Version 2017.1a

The following issues and enhancement requests have been addressed in the 2017.1a release:

HDL Designer Series

The following issues and enhancement requests have been addressed in HDL Designer Series 2017.1a release:

- **DR 517869**
  Description: Request to fix an issue in running version management operations in the logical objects view. Operations fail when all objects associated with a design unit are not selected, yet, HDL Designer Series reports that operations are successful.
- **DR 1063918**
  Description: Request to add an option in the Subversion workspace commit operation that allows adding lock properties for added files when adding all sub-directories beneath a directory.
- **DR 1085999**
  Description: Request to enhance the process of changing file names for files under Subversion.

- **DR 1125254**

  Description: Request to fix an issue in which converting blocks to components, while using Subversion, raises errors in certain cases.

- **DR 1149710**

  Description: Request to fix the mechanism of converting blocks to components in Subversion.

- **DR 1191893**

  Description: Request to fix Subversion update errors raised on committing empty directories.

- **DR 1198092**

  Description: Request to restore the ability to create protected libraries in batch mode when using the -point mode.

- **DR 1223217**

  Description: Request to have an option to specify the names of Vivado IP cores to be imported prior to their import process.

- **DR 1288786**

  Description: Request to support VHDL 2008 Tool Directives in both HDL Designer Series and DesignChecker.

- **DR 1291972**

  Description: Request to fix a crash that occurs on converting from HDL to graphics.

- **DR 1292867**

  Description: Request to enhance the Xilinx Vivado flow to support SystemVerilog top-level simulation files.

- **DR 1295190**

  Description: Request to fix a crash that occurs on converting VHDL code to a state machine diagram.

- **DR 1299309**

  Description: Request to support Xilinx Vivado 2017.3.

- **DR 1299372**

  Description: Request to fix an issue in which Xilinx Vivado fails when importing IP. The following message is raised: “can’t use non-numeric string as operand of ‘!’.”

DesignChecker

The following issues and enhancement requests have been addressed in DesignChecker 2017.1a release:

- **DR 1156910**

Description: Request to fix an issue in which DesignChecker synthesis incorrectly raises an error for a VHDL function return.

- **DR 1213189**

  Description: Request to enhance the exclusions capability to allow applying synthesis pragmas at parsing level.

- **DR 1225117**

  Description: Request to restore the behavior of the Structural Core base rule so that it checks the top-level design unit only. The Structural Core base rule incorrectly raises violations for instances.

- **DR 1239996**

  Description: Request to fix a false error raised by DesignChecker due to a required VHDL package.

- **DR 1262116**

  Description: Request to allow the missing declaration flow to generate missing architectures when multiple architectures are available for the same entity.

- **DR 1266032**

  Description: Request to fix a syntax error raised by DesignChecker for a package that is actually available in the library.

- **DR 1290318**

  Description: Request to fix an elaboration error reported by DesignChecker when using the DesignChecker batch *.ini* flow.

- **DR 1290663**

  Description: Request to fix an issue in DesignChecker in which the tool reports “No Policy” in the **Results** tab after loading a *.tbc* file using the default policy.

- **DR 1290911**

  Description: Request to fix an application error raised by DesignPad on opening a source file from DesignChecker after loading a *.tbc* file.

- **DR 1294389**

  Description: Request to fix an elaboration error raised when a generic has no default value.

- **HDS-4075**

  Description: Request to allow DesignChecker to load *.tbc* result files even if the configured rules do not exist.

- **HDS-4234**

  Description: Request to fix DesignChecker to show the correct rule severity of violations in a loaded *.tbc* file based on the ruleset used while running analysis.

SystemVerilog-VHDL Assistant

The following issues and enhancement requests have been addressed in SystemVerilog-VHDL Assistant 2017.1a release:

- **DR 1091081**
  Description: Request to fix corrupted syntax highlighting between Verilog ticks.
- **DR 1264342**
  Description: Request to ensure the consistency of SystemVerilog-VHDL Assistant syntax errors. SystemVerilog-VHDL Assistant raises syntax errors in a project only when it is the second project opened in the same SystemVerilog-VHDL Assistant session.
- **DR 1291578**
  Description: Request to fix a Java exception error raised on importing a design.
- **DR 1294584**
  Description: Request to fix an issue in which a target is not created when a build variable is defined in the build command but is not defined in the Makefile.
- **DR 1300539**
  Description: Request to fix the ability to change font settings in SystemVerilog-VHDL Assistant preferences.
- **HDS-3883**
  Description: Request to simplify Makefile target names.
- **HDS-3894**
  Description: Request to support running DesignChecker flow on a subhierarchy in SystemVerilog-VHDL Assistant.
- **HDS-4150**
  Description: Request to keep non-existing files in SystemVerilog-VHDL Assistant project files instead of having non-existing files automatically removed.

Software Version 2017.1

The following issues and enhancement requests have been addressed in the 2017.1 release:

HDL Designer Series

The following issues and enhancement requests have been addressed in HDL Designer Series 2017.1 release:

- **DR 1125256**
  Description: Request to fix a misleading Subversion message raised on saving a view without changes.

- **DR 1137940**

  Description: Request to support the Vivado 2015.1 core container feature.

- **DR 1139103**

  Description: Request to fix an issue in which an error is raised on running the Subversion Commit operation on libraries without version management mappings.

- **DR 1166493**

  Description: Request to fix a syntax parsing error in HDS 2015.1a for valid code containing reference to ‘event attribute.

- **DR 1195410**

  Description: Request to disallow edits in embedded block diagrams when the parent diagram is locked as read-only using Subversion.

- **DR 1233387**

  Description: Request to allow the Vivado flow to create a file list in non-project mode.

- **DR 1234389**

  Description: Request to unify the versions of JAVA used in the HDS installation.

- **DR 1244681**

  Description: Request to fix an issue in which the -do file of ModelSim/Questa is not added to the *hds_args.tmp* file when the *.fpf* file for top-level is read-only.

- **DR 1247198**

  Description: Request to document the *.cache.dat* file and all file types used in HDL Designer Series.

- **DR 1255804**

  Description: Request to modify the behavior of the “Add Library to Library Search Path” feature to not add IP libraries to the search path when compiling/mapping Vivado libraries.

- **DR 1255827**

  Description: Request to check that *modelsim.ini* in Vivado is writable before making the mappings.

- **DR 1258179**

  Description: Request to fix an issue in which HDS raises false warnings during generation when all checks are enabled in the Main Settings dialog box.

- **DR 1258218**

  Description: Request to display the project name in the header of HDS graphical editors (similar to the Design Manager).

- **DR 1260302**

  Description: Request to update the description of the setupHdlImport API command in the Tcl Command Reference.

- **DR 1260771**
  Description: Request to support the Libero V11.7 SP3 new supported package.
- **DR 1263754**
  Description: Request to change the message re-direction from STDERR to STDOUT in the HDS wrapper script on Linux.
- **DR 1264294**
  Description: Request to fix an issue in which HDS allows only one atomic license to be checked out when running in batch while the DISPLAY variable is unset.
- **DR 1264483**
  Description: Request to fix ModuleWare **Details** to open the corresponding help page correctly.
- **DR 1265907**
  Description: Request to fix an issue in which when an HDS design contains multiple FPGAs, *glbl* is called more than once on the vsim command line, hence, causing a failure while loading to Questa.
- **DR 1268881**
  Description: Request to fix an issue in which HDS cannot identify a locally mounted drive when opening a project.
- **DR 1270210**
  Description: Request to modify the HDS_SVN_COMMAND_FILE_LIMIT to be set automatically.
- **DR 1273653**
  Description: Request to remove information from the user manual about specifying relative locations for the library path which is no longer supported.
- **DR 1275504**
  Description: Request the ability to communicate the dialect of HDS VHDL files to Vivado.
- **DR 1279584**
  Description: Request to support the Libero V11.8 new supported package.

DesignChecker

The following issues and enhancement requests have been addressed in DesignChecker 2017.1 release:

- **DR 907784**
  Description: Request to fix a hang in DesignChecker that occurs when performing Deep Analysis on a module.
- **DR 908141**

Description: Request to fix a hang in DesignChecker that occurs due to a series of FOR loops.

- **DR 1119642**

  Description: Request to fix an issue in which a DesignChecker synthesis check fails to run properly.

- **DR 1129815**

  Description: Request to fix a crash in DesignChecker RTLC engine that occurs on running Deep Analysis.

- **DR 1192265**

  Description: Request to allow DesignChecker to verify that an FPGA/ASIC input has a two-stage synchronizer before driving other logic.

- **DR 1209670**

  Description: Request to enhance DesignChecker to detect always true expressions.

- **DR 1212201**

  Description: Request to allow DesignChecker to detect pipelined signals.

- **DR 1214170**

  Description: Request to fix a DesignChecker synthesis check failure resulting from memory allocation failure.

- **DR 1230842**

  Description: Request to fix an issue in which DesignChecker provides partial results and raises the following error: “Fatal 7003: Segmentation violation.”

- **DR 1236960**

  Description: Request to document the disableExportExcludedViolations and enableExportExcludedViolations API commands.

- **DR 1238622**

  Description: Request to enhance DesignChecker to flag a “dangling else” for nested If statements.

- **DR 1249023**

  Description: Request to fix an issue in which DesignChecker reports “unsupported language dialect” for a SystemVerilog file with extension *.behV*.

- **DR 1255830**

  Description: Request to document the ‘define parameter available in the State Encoding Style dialog box.

- **DR 1256921**

  Description: Request to fix an issue in which DesignChecker raises a syntax error for valid VHDL code that compiles correctly in Questa.

- **DR 1257687**

  Description: Request to allow DesignChecker to check that there are no flip-flops having both asynchronous preset and clear signals.

- **DR 1257900**

  Description: Request to fix a crash in DesignChecker that occurs on saving a justification for a disabled rule.

- **DR 1261907**

  Description: Request to fix the File Name base rule documentation to use a correct file name pattern in the example.

- **DR 1262441**

  Description: Request to fix an issue in which DesignChecker raises the syntax error “Cannot find source file <path>” due to file handles leak, although the file(s) exists.

- **DR 1266751**

  Description: Request to fix an issue in which DesignChecker produces failures on a specific design.

- **DR 1271757**

  Description: Request to fix an issue in which running DesignChecker on a specific design results in segmentation violation and deep analysis failure.

- **DR 1286039**

  Description: Request to add API commands in the DesignChecker batch flow to allow setting the gate level limit.

- **DR 1286588**

  Description: Request to enhance the DesignChecker API command importFileList to support environment variables in file lists.

SystemVerilog-VHDL Assistant

The following issues and enhancement requests have been addressed in SystemVerilog-VHDL Assistant 2017.1 release:

- **DR 1228527**

  Description: Request to support the ability to run external tools from SystemVerilog-VHDL Assistant.

- **DR 1229049**

  Description: Request to fix SV_ROOT which incorrectly points to a 32-bit path even when preferences point to a 64-bit tree.

- **DR 1232638**

  Description: Request to allow SVA makefile to support “referenced” packages without explicit import statements.

- **DR 1233577**

  Description: Request to fix a crash in SystemVerilog-VHDL Assistant that occurs on adding a build library.

- **DR 1239668**

  Description: Request to handle miscellaneous fixes in the *SystemVerilog-VHDL Assistant API Reference Manual*.

- **DR 1244924**

  Description: Request to fix the reload project feature to maintain the default top unit set by the user.

- **DR 1244927**

  Description: Request to fix the behavior of the reload feature in both GUI and API commands to be consistent in handling the default top unit.

- **DR 1245925**

  Description: Request to allow new files created using the Extend Class functionality to use the default template.

- **DR 1247937**

  Description: Request to disallow dropping packages (header/body) too FFT VHDL files.

- **DR 1253506**

  Description: Request to support importing design and vendor libraries in SystemVerilog-VHDL Assistant.

- **DR 1257585**

  Description: Request to investigate broken links in the Help of SystemVerilog-VHDL Assistant on Linux.

- **DR 1258705**

  Description: Request to fix issues in the installation of subclipse on Linux for SystemVerilog-VHDL Assistant and in accessing Subversion (SVN) preferences.

- **DR 1258748**

  Description: Request to fix content in the SystemVerilog-VHDL Assistant Command Categories section in the *SystemVerilog-VHDL Assistant API Reference Manual*.

- **DR 1264476**

  Description: Request to fix an issue in which SystemVerilog-VHDL Assistant creates hard paths if relative and soft paths are enabled.

- **DR 1264479**

  Description: Request to modify the File Browser dialog boxes to keep the last used location or to add a preference to set the default location.

- **DR 1269919**

Description: Request to fix an issue in which upper case letters in SystemVerilog module names instantiated in VDHL cause rules in the generated makefile to be inconsistent.

- **DR 1270211**
  Description: Request to fix an issue in which QVIP license errors are raised when Questa is invoked from SystemVerilog-VHDL Assistant.

- **DR 1287638**
  Description: Request to add a project setting that allows turning off the automatic setting of the default top.

Register Assistant

The following issues and enhancement requests have been addressed in Register Assistant 4.9 release:

- **DR 1162366**
  Description: Request to update *Register Assistant User Manual* to clarify the behavior of RTL generation when a memory is specified in the input.

- **DR 1264588**
  Description: Request to fix an issue in which the IP-XACT importer interprets registers incorrectly.

All numbers refer to the ClearQuest defect tracking system. For clarity, the prefix *DR* represents the ClearQuest database prefix *dts01* and other leading zeros are omitted.

User Documentation

The following manuals are provided with this release:

Start Here Guide for the HDL Designer Series	Software Version 2018.1
HDL Designer Series User Manual	Software Version 2018.1
Graphical Editors User Manual	Software Version 2018.1
State Machine Editors User Manual	Software Version 2018.1
Interface-Based Design Tutorial	Software Version 2018.1
Design Exploration Tutorial	Software Version 2018.1
HDS Language Support Guide	Software Version 2018.1
HDL Designer Series Tcl Reference Manual	Software Version 2018.1
DesignChecker User Guide	Software Version 2018.1
DesignChecker API Reference Manual	Software Version 2018.1
DesignChecker Tutorial	Software Version 2018.1

DesignChecker Release Notes	Software Version 2018.1
Using DesignChecker with HDL Designer Series	Software Version 2018.1
DesignPad Text Editor User Guide	Software Version 2.72
ModuleWare Reference Guide	Library Version 1.12
Register Assistant User Manual	Software Version 5.0
Register Assistant Release Notes	Software Version 5.0
Using Register Assistant with HDL Designer Series	Software Version 2018.1
SystemVerilog-VHDL Assistant Reference Manual	Software Version 2018.1
Using SystemVerilog-VHDL Assistant with HDL Designer Series	Software Version 2018.1
Using DesignChecker with SystemVerilog-VHDL Assistant	Software Version 2018.1

Tracking Service Requests, DRs, and ERs

If you are a registered Support Center user, you can always view the status of your own Service Requests, including the detailed status of any attached Defect Report (DR) or Enhancement Request (ER). You can also view all Service Requests for your site, including all associated DRs and ERs.

In addition, all publicly accessible DRs and ERs are available on Support Center. If you would like to know the status of a DR or ER that is not attached to any of your or your company's Service Requests, go to the "Service Requests" page on Support Center and use the search field to type your product.

Note

Some defects may not be made public for various technical or business reasons; this is determined on a case-by-case basis.

To be kept informed of the progress of a particular DR or ER, open a service request and indicate the DR or ER number you are interested in.

Chapter 4
Browser Settings

Verify that your browser version is supported and that you have the required browser settings for accessing and viewing the Mentor Documentation System (including InfoHub), and Support Center.

Tip: The InfoHub and HTML documents will not fully function unless the browser settings enable JavaScript to run. Without JavaScript enabled, the InfoHub and HTML documents fall back to a Compatibility Mode, with only single navigation and no search capability.

If you are using one of the following unsupported browsers, follow the remedy.

Unsupported Browsers	Remedy
Firefox 1.x	Upgrade to version 3.x or newer.
Internet Explorer 5.x, 6.x, 7.x	Upgrade to version 8.x or newer. You can also use Microsoft Edge.
Mozilla 1.x	No longer supported by Mozilla, upgrade to Firefox.
Netscape 4.x, 6.x, 7.x, 8.x, and 9.x	Upgrade to Firefox.
Opera 6.x, 7.x, 8.x, and 9.x	Upgrade to the 10.x or newer.

Viewing PDF files — PDF files do not fully function when viewed within a web browser due to browser plug-in security restrictions. Use the HTML version of the documentation to fully navigate and search. You can also navigate to the documentation tree and view the PDFs using a PDF Viewer, such as Adobe Reader.

Following is a list of supported browsers for viewing the HTML documentation:

- Edge
- Internet Explorer 8.x, 9.x, 10.x, and Newer
- Firefox 4.x and Newer
- Chrome 9 and Newer
- Safari 5.x and 6.x

- Opera 10x through 12x

Edge

Set up Edge options to properly access and view the InfoHub and Support Center.

Procedure

At this time, no action is needed within Edge to set options in order to view or use the InfoHub and HTML documentation.

Internet Explorer 8.x, 9.x, 10.x, and Newer

Set up Internet Explorer options to properly access and view the InfoHub and Support Center.

Note

Internet Explorer 7.x uses an older generation JavaScript interpreter. Thus, it is significantly slower loading the search data and navigating around the InfoHub and HTML documents. It is recommended that you update to a newer version of Internet Explorer, Edge, Firefox, or Chrome.

Procedure

1. Choose **Tools > Internet Options** menu item, then set the options.
2. If you are running Windows 7, Vista, or Windows XP Service Pack 2 or later, perform the following: on the **Advanced** tab, select “Allow active content to run in files on My Computer” in order for the InfoHub and HTML documents to fully function.

   If you do not want to change the security setting for the active content on My Computer, you can alternately host the documentation on an internal web-server.
3. On the **Security** tab, select the “Internet” Web content zone, then click **Custom Level**. “Enable” the following Scripting options: Active Scripting and Scripting of Java Applets. Under **User Authentication > Logon**, choose either “Automatic logon only in Intranet zone” or “Prompt for user name and password”. Click **OK**.
4. On the **Security** tab, select the “Local intranet” Web content zone, then duplicate the settings made in step 2.
5. On the **Privacy** tab, set the Automatic cookie handling setting to a level that will accept session cookies (try Medium), or use the Advanced options to override automatic settings. Session cookies are required for opening a Service Request on Support Center.
6. Click **OK**.

Firefox 4.x and Newer

Set up Firefox options to properly access and view the InfoHub and Support Center.

Prerequisite

If you are using a version of Firefox that is in the range of v4 to v22, you need to confirm your settings. Otherwise, if you are using Firefox v23 and newer, it functions with the default settings.

Procedure

1. Choose **Firefox** menu and then the **Options** menu item to set the options.
2. For older versions, under the Content option, verify that “Enable JavaScript” is selected.
3. Under the Privacy option, choose the History dropdown item “Use custom settings for history.” Choose “Accept cookies from sites,” if not already selected.
4. Click **OK**.

Chrome 9 and Newer

Set up Chrome options to properly access and view the InfoHub and Support Center.

Note

When using Google Chrome to access Mentor HTML documents from the local file system (file://), inter-frame communication with JavaScript is disabled for security purposes. Most features of the HTML documents are still functional, including navigation and search. The following features that depend on inter-frame communication are disabled: open to PDF topic, print topic, breadcrumbs bar, resizing of text, highlighting of search results, and TOC highlighting in the left sidebar. To enable all features, you can host the documentation on an HTTP server or use Firefox.

Procedure

1. Click **Customize and control Google Chrome** (Menu button), then set the options.
2. Choose **Settings** and click on the “Show advanced settings” link at the bottom of the page, or **Options** > **Under the Hood** > **Privacy** item, depending on your version of Chrome.
3. Scroll to Privacy section and click **Content settings**.
4. Under JavaScript, verify that “Allow all sites to run JavaScript,” is selected.
5. Click **Done** or the **X** in the upper right corner to accept the changes.

Safari 5.x and 6.x

Set up Safari options to properly access and view the InfoHub and Support Center.

Procedure

1. Choose **general Safari settings** (Gear button) > **Preferences** menu item, then set the options.
2. Choose the **Security** tab.
3. Under Web Content, set “Enable Javascript”.
4. Click the **X** in the upper right corner to accept the changes.

Opera 10x through 12x

Set up Opera options to properly access and view the InfoHub and Support Center.

Procedure

1. Choose **Tools** > **Preferences** menu item, then set the options.
2. Open the **Advanced** tab, and under the Content item, verify that the “Enable JavaScript” option is selected.
3. In the **Advanced** tab, click on the **Style options** button and verify that the following options are enabled: “Enable frames” and “Enable inline frames.” Click **OK**.
4. Under the **Cookies** item, select “Accept cookies.”
5. Click **OK**.

End-User License Agreement

The latest version of the End-User License Agreement is available on-line at:
www.mentor.com/eula

IMPORTANT INFORMATION

USE OF ALL SOFTWARE IS SUBJECT TO LICENSE RESTRICTIONS. CAREFULLY READ THIS LICENSE AGREEMENT BEFORE USING THE PRODUCTS. USE OF SOFTWARE INDICATES CUSTOMER'S COMPLETE AND UNCONDITIONAL ACCEPTANCE OF THE TERMS AND CONDITIONS SET FORTH IN THIS AGREEMENT. ANY ADDITIONAL OR DIFFERENT PURCHASE ORDER TERMS AND CONDITIONS SHALL NOT APPLY.

END-USER LICENSE AGREEMENT ("Agreement")

This is a legal agreement concerning the use of Software (as defined in Section 2) and hardware (collectively "Products") between the company acquiring the Products ("Customer"), and the Mentor Graphics entity that issued the corresponding quotation or, if no quotation was issued, the applicable local Mentor Graphics entity ("Mentor Graphics"). Except for license agreements related to the subject matter of this license agreement which are physically signed by Customer and an authorized representative of Mentor Graphics, this Agreement and the applicable quotation contain the parties' entire understanding relating to the subject matter and supersede all prior or contemporaneous agreements. If Customer does not agree to these terms and conditions, promptly return or, in the case of Software received electronically, certify destruction of Software and all accompanying items within five days after receipt of Software and receive a full refund of any license fee paid.

1. **ORDERS, FEES AND PAYMENT.**

   1.1. To the extent Customer (or if agreed by Mentor Graphics, Customer's appointed third party buying agent) places and Mentor Graphics accepts purchase orders pursuant to this Agreement (each an "Order"), each Order will constitute a contract between Customer and Mentor Graphics, which shall be governed solely and exclusively by the terms and conditions of this Agreement, any applicable addenda and the applicable quotation, whether or not those documents are referenced on the Order. Any additional or conflicting terms and conditions appearing on an Order or presented in any electronic portal or automated order management system, whether or not required to be electronically accepted, will not be effective unless agreed in writing and physically signed by an authorized representative of Customer and Mentor Graphics.

   1.2. Amounts invoiced will be paid, in the currency specified on the applicable invoice, within 30 days from the date of such invoice. Any past due invoices will be subject to the imposition of interest charges in the amount of one and one-half percent per month or the applicable legal rate currently in effect, whichever is lower. Prices do not include freight, insurance, customs duties, taxes or other similar charges, which Mentor Graphics will state separately in the applicable invoice. Unless timely provided with a valid certificate of exemption or other evidence that items are not taxable, Mentor Graphics will invoice Customer for all applicable taxes including, but not limited to, VAT, GST, sales tax, consumption tax and service tax. Customer will make all payments free and clear of, and without reduction for, any withholding or other taxes; any such taxes imposed on payments by Customer hereunder will be Customer's sole responsibility. If Customer appoints a third party to place purchase orders and/or make payments on Customer's behalf, Customer shall be liable for payment under Orders placed by such third party in the event of default.

   1.3. All Products are delivered FCA factory (Incoterms 2010), freight prepaid and invoiced to Customer, except Software delivered electronically, which shall be deemed delivered when made available to Customer for download. Mentor Graphics retains a security interest in all Products delivered under this Agreement, to secure payment of the purchase price of such Products, and Customer agrees to sign any documents that Mentor Graphics determines to be necessary or convenient for use in filing or perfecting such security interest. Mentor Graphics' delivery of Software by electronic means is subject to Customer's provision of both a primary and an alternate e-mail address.

2. **GRANT OF LICENSE.** The software installed, downloaded, or otherwise acquired by Customer under this Agreement, including any updates, modifications, revisions, copies, documentation, setup files and design data ("Software") are copyrighted, trade secret and confidential information of Mentor Graphics or its licensors, who maintain exclusive title to all Software and retain all rights not expressly granted by this Agreement. Except for Software that is embeddable ("Embedded Software"), which is licensed pursuant to separate embedded software terms or an embedded software supplement, Mentor Graphics grants to Customer, subject to payment of applicable license fees, a nontransferable, nonexclusive license to use Software solely: (a) in machine-readable, object-code form (except as provided in Subsection 4.2); (b) for Customer's internal business purposes; (c) for the term of the license; and (d) on the computer hardware and at the site authorized by Mentor Graphics. A site is restricted to a one-half mile (800 meter) radius. Customer may have Software temporarily used by an employee for telecommuting purposes from locations other than a Customer office, such as the employee's residence, an airport or hotel, provided that such employee's primary place of employment is the site where the Software is authorized for use. Mentor Graphics' standard policies and programs, which vary depending on Software, license fees paid or services purchased, apply to the following: (a) relocation of Software; (b) use of Software, which may be limited, for example, to execution of a single session by a single user on the authorized hardware or for a restricted period of time (such limitations may be technically implemented through the use of authorization codes or similar devices); and (c) support services provided, including eligibility to receive telephone support, updates, modifications, and revisions. For the avoidance of doubt, if Customer provides any feedback or requests any change or enhancement to Products, whether in the course of receiving support or consulting services, evaluating Products, performing beta testing or otherwise, any inventions, product improvements, modifications or developments made by Mentor Graphics (at Mentor Graphics' sole discretion) will be the exclusive property of Mentor Graphics.

3. **BETA CODE.**

3.1. Portions or all of certain Software may contain code for experimental testing and evaluation (which may be either alpha or beta, collectively "Beta Code"), which may not be used without Mentor Graphics' explicit authorization. Upon Mentor Graphics' authorization, Mentor Graphics grants to Customer a temporary, nontransferable, nonexclusive license for experimental use to test and evaluate the Beta Code without charge for a limited period of time specified by Mentor Graphics. Mentor Graphics may choose, at its sole discretion, not to release Beta Code commercially in any form.

3.2. If Mentor Graphics authorizes Customer to use the Beta Code, Customer agrees to evaluate and test the Beta Code under normal conditions as directed by Mentor Graphics. Customer will contact Mentor Graphics periodically during Customer's use of the Beta Code to discuss any malfunctions or suggested improvements. Upon completion of Customer's evaluation and testing, Customer will send to Mentor Graphics a written evaluation of the Beta Code, including its strengths, weaknesses and recommended improvements.

3.3. Customer agrees to maintain Beta Code in confidence and shall restrict access to the Beta Code, including the methods and concepts utilized therein, solely to those employees and Customer location(s) authorized by Mentor Graphics to perform beta testing. Customer agrees that any written evaluations and all inventions, product improvements, modifications or developments that Mentor Graphics conceived or made during or subsequent to this Agreement, including those based partly or wholly on Customer's feedback, will be the exclusive property of Mentor Graphics. Mentor Graphics will have exclusive rights, title and interest in all such property. The provisions of this Subsection 3.3 shall survive termination of this Agreement.

4. **RESTRICTIONS ON USE.**

4.1. Customer may copy Software only as reasonably necessary to support the authorized use. Each copy must include all notices and legends embedded in Software and affixed to its medium and container as received from Mentor Graphics. All copies shall remain the property of Mentor Graphics or its licensors. Except for Embedded Software that has been embedded in executable code form in Customer's product(s), Customer shall maintain a record of the number and primary location of all copies of Software, including copies merged with other software, and shall make those records available to Mentor Graphics upon request. Customer shall not make Products available in any form to any person other than Customer's employees and on-site contractors, excluding Mentor Graphics competitors, whose job performance requires access and who are under obligations of confidentiality. Customer shall take appropriate action to protect the confidentiality of Products and ensure that any person permitted access does not disclose or use Products except as permitted by this Agreement. Customer shall give Mentor Graphics written notice of any unauthorized disclosure or use of the Products as soon as Customer becomes aware of such unauthorized disclosure or use. Customer acknowledges that Software provided hereunder may contain source code which is proprietary and its confidentiality is of the highest importance and value to Mentor Graphics. Customer acknowledges that Mentor Graphics may be seriously harmed if such source code is disclosed in violation of this Agreement. Except as otherwise permitted for purposes of interoperability as specified by applicable and mandatory local law, Customer shall not reverse-assemble, disassemble, reverse-compile, or reverse-engineer any Product, or in any way derive any source code from Software that is not provided to Customer in source code form. Log files, data files, rule files and script files generated by or for the Software (collectively "Files"), including without limitation files containing Standard Verification Rule Format ("SVRF") and Tcl Verification Format ("TVF") which are Mentor Graphics' trade secret and proprietary syntaxes for expressing process rules, constitute or include confidential information of Mentor Graphics. Customer may share Files with third parties, excluding Mentor Graphics competitors, provided that the confidentiality of such Files is protected by written agreement at least as well as Customer protects other information of a similar nature or importance, but in any case with at least reasonable care. Customer may use Files containing SVRF or TVF only with Mentor Graphics products. Under no circumstances shall Customer use Products or Files or allow their use for the purpose of developing, enhancing or marketing any product that is in any way competitive with Products, or disclose to any third party the results of, or information pertaining to, any benchmark.

4.2. If any Software or portions thereof are provided in source code form, Customer will use the source code only to correct software errors and enhance or modify the Software for the authorized use, or as permitted for Embedded Software under separate embedded software terms or an embedded software supplement. Customer shall not disclose or permit disclosure of source code, in whole or in part, including any of its methods or concepts, to anyone except Customer's employees or on-site contractors, excluding Mentor Graphics competitors, with a need to know. Customer shall not copy or compile source code in any manner except to support this authorized use.

4.3. Customer agrees that it will not subject any Product to any open source software ("OSS") license that conflicts with this Agreement or that does not otherwise apply to such Product.

4.4. Customer may not assign this Agreement or the rights and duties under it, or relocate, sublicense, or otherwise transfer the Products, whether by operation of law or otherwise ("Attempted Transfer"), without Mentor Graphics' prior written consent and payment of Mentor Graphics' then-current applicable relocation and/or transfer fees. Any Attempted Transfer without Mentor Graphics' prior written consent shall be a material breach of this Agreement and may, at Mentor Graphics' option, result in the immediate termination of the Agreement and/or the licenses granted under this Agreement. The terms of this Agreement, including without limitation the licensing and assignment provisions, shall be binding upon Customer's permitted successors in interest and assigns.

4.5. The provisions of this Section 4 shall survive the termination of this Agreement.

5. **SUPPORT SERVICES.** To the extent Customer purchases support services, Mentor Graphics will provide Customer with updates and technical support for the Products, at the Customer site(s) for which support is purchased, in accordance with Mentor Graphics' then current End-User Support Terms located at http://supportnet.mentor.com/supportterms.

6. **OPEN SOURCE SOFTWARE.** Products may contain OSS or code distributed under a proprietary third party license agreement, to which additional rights or obligations ("Third Party Terms") may apply. Please see the applicable Product documentation (including license files, header files, read-me files or source code) for details. In the event of conflict between the terms of this Agreement

(including any addenda) and the Third Party Terms, the Third Party Terms will control solely with respect to the OSS or third party code. The provisions of this Section 6 shall survive the termination of this Agreement.

7. **LIMITED WARRANTY.**

7.1. Mentor Graphics warrants that during the warranty period its standard, generally supported Products, when properly installed, will substantially conform to the functional specifications set forth in the applicable user manual. Mentor Graphics does not warrant that Products will meet Customer's requirements or that operation of Products will be uninterrupted or error free. The warranty period is 90 days starting on the 15th day after delivery or upon installation, whichever first occurs. Customer must notify Mentor Graphics in writing of any nonconformity within the warranty period. For the avoidance of doubt, this warranty applies only to the initial shipment of Software under an Order and does not renew or reset, for example, with the delivery of (a) Software updates or (b) authorization codes or alternate Software under a transaction involving Software re-mix. This warranty shall not be valid if Products have been subject to misuse, unauthorized modification, improper installation or Customer is not in compliance with this Agreement. MENTOR GRAPHICS' ENTIRE LIABILITY AND CUSTOMER'S EXCLUSIVE REMEDY SHALL BE, AT MENTOR GRAPHICS' OPTION, EITHER (A) REFUND OF THE PRICE PAID UPON RETURN OF THE PRODUCTS TO MENTOR GRAPHICS OR (B) MODIFICATION OR REPLACEMENT OF THE PRODUCTS THAT DO NOT MEET THIS LIMITED WARRANTY. MENTOR GRAPHICS MAKES NO WARRANTIES WITH RESPECT TO: (A) SERVICES; (B) PRODUCTS PROVIDED AT NO CHARGE; OR (C) BETA CODE; ALL OF WHICH ARE PROVIDED "AS IS."

7.2. THE WARRANTIES SET FORTH IN THIS SECTION 7 ARE EXCLUSIVE. NEITHER MENTOR GRAPHICS NOR ITS LICENSORS MAKE ANY OTHER WARRANTIES EXPRESS, IMPLIED OR STATUTORY, WITH RESPECT TO PRODUCTS PROVIDED UNDER THIS AGREEMENT. MENTOR GRAPHICS AND ITS LICENSORS SPECIFICALLY DISCLAIM ALL IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE AND NON-INFRINGEMENT OF INTELLECTUAL PROPERTY.

8. **LIMITATION OF LIABILITY.** TO THE EXTENT PERMITTED UNDER APPLICABLE LAW, IN NO EVENT SHALL MENTOR GRAPHICS OR ITS LICENSORS BE LIABLE FOR INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES (INCLUDING LOST PROFITS OR SAVINGS) WHETHER BASED ON CONTRACT, TORT OR ANY OTHER LEGAL THEORY, EVEN IF MENTOR GRAPHICS OR ITS LICENSORS HAVE BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. IN NO EVENT SHALL MENTOR GRAPHICS' OR ITS LICENSORS' LIABILITY UNDER THIS AGREEMENT EXCEED THE AMOUNT RECEIVED FROM CUSTOMER FOR THE HARDWARE, SOFTWARE LICENSE OR SERVICE GIVING RISE TO THE CLAIM. IN THE CASE WHERE NO AMOUNT WAS PAID, MENTOR GRAPHICS AND ITS LICENSORS SHALL HAVE NO LIABILITY FOR ANY DAMAGES WHATSOEVER. THE PROVISIONS OF THIS SECTION 8 SHALL SURVIVE THE TERMINATION OF THIS AGREEMENT.

9. **THIRD PARTY CLAIMS.**

9.1. Customer acknowledges that Mentor Graphics has no control over the testing of Customer's products, or the specific applications and use of Products. Mentor Graphics and its licensors shall not be liable for any claim or demand made against Customer by any third party, except to the extent such claim is covered under Section 10.

9.2. In the event that a third party makes a claim against Mentor Graphics arising out of the use of Customer's products, Mentor Graphics will give Customer prompt notice of such claim. At Customer's option and expense, Customer may take sole control of the defense and any settlement of such claim. Customer WILL reimburse and hold harmless Mentor Graphics for any LIABILITY, damages, settlement amounts, costs and expenses, including reasonable attorney's fees, incurred by or awarded against Mentor Graphics or its licensors in connection with such claims.

9.3. The provisions of this Section 9 shall survive any expiration or termination of this Agreement.

10. **INFRINGEMENT.**

10.1. Mentor Graphics will defend or settle, at its option and expense, any action brought against Customer in the United States, Canada, Japan, or member state of the European Union which alleges that any standard, generally supported Product acquired by Customer hereunder infringes a patent or copyright or misappropriates a trade secret in such jurisdiction. Mentor Graphics will pay costs and damages finally awarded against Customer that are attributable to such action. Customer understands and agrees that as conditions to Mentor Graphics' obligations under this section Customer must: (a) notify Mentor Graphics promptly in writing of the action; (b) provide Mentor Graphics all reasonable information and assistance to settle or defend the action; and (c) grant Mentor Graphics sole authority and control of the defense or settlement of the action.

10.2. If a claim is made under Subsection 10.1 Mentor Graphics may, at its option and expense: (a) replace or modify the Product so that it becomes noninfringing; (b) procure for Customer the right to continue using the Product; or (c) require the return of the Product and refund to Customer any purchase price or license fee paid, less a reasonable allowance for use.

10.3. Mentor Graphics has no liability to Customer if the action is based upon: (a) the combination of Software or hardware with any product not furnished by Mentor Graphics; (b) the modification of the Product other than by Mentor Graphics; (c) the use of other than a current unaltered release of Software; (d) the use of the Product as part of an infringing process; (e) a product that Customer makes, uses, or sells; (f) any Beta Code or Product provided at no charge; (g) any software provided by Mentor Graphics' licensors who do not provide such indemnification to Mentor Graphics' customers; (h) OSS, except to the extent that the infringement is directly caused by Mentor Graphics' modifications to such OSS; or (i) infringement by Customer that is deemed willful. In the case of (i), Customer shall reimburse Mentor Graphics for its reasonable attorney fees and other costs related to the action.

10.4. THIS SECTION 10 IS SUBJECT TO SECTION 8 ABOVE AND STATES THE ENTIRE LIABILITY OF MENTOR GRAPHICS AND ITS LICENSORS, AND CUSTOMER'S SOLE AND EXCLUSIVE REMEDY, FOR DEFENSE, SETTLEMENT AND DAMAGES, WITH RESPECT TO ANY ALLEGED PATENT OR COPYRIGHT INFRINGEMENT OR TRADE SECRET MISAPPROPRIATION BY ANY PRODUCT PROVIDED UNDER THIS AGREEMENT.

11. **TERMINATION AND EFFECT OF TERMINATION.**

11.1. If a Software license was provided for limited term use, such license will automatically terminate at the end of the authorized term. Mentor Graphics may terminate this Agreement and/or any license granted under this Agreement immediately upon written notice if Customer: (a) exceeds the scope of the license or otherwise fails to comply with the licensing or confidentiality provisions of this Agreement, or (b) becomes insolvent, files a bankruptcy petition, institutes proceedings for liquidation or winding up or enters into an agreement to assign its assets for the benefit of creditors. For any other material breach of any provision of this Agreement, Mentor Graphics may terminate this Agreement and/or any license granted under this Agreement upon 30 days written notice if Customer fails to cure the breach within the 30 day notice period. Termination of this Agreement or any license granted hereunder will not affect Customer's obligation to pay for Products shipped or licenses granted prior to the termination, which amounts shall be payable immediately upon the date of termination.

11.2. Upon termination of this Agreement, the rights and obligations of the parties shall cease except as expressly set forth in this Agreement. Upon termination of this Agreement and/or any license granted under this Agreement, Customer shall ensure that all use of the affected Products ceases, and shall return hardware and either return to Mentor Graphics or destroy Software in Customer's possession, including all copies and documentation, and certify in writing to Mentor Graphics within ten business days of the termination date that Customer no longer possesses any of the affected Products or copies of Software in any form.

12. **EXPORT.** The Products provided hereunder are subject to regulation by local laws and European Union ("E.U.") and United States ("U.S.") government agencies, which prohibit export, re-export or diversion of certain products, information about the products, and direct or indirect products thereof, to certain countries and certain persons. Customer agrees that it will not export or re-export Products in any manner without first obtaining all necessary approval from appropriate local, E.U. and U.S. government agencies. If Customer wishes to disclose any information to Mentor Graphics that is subject to any E.U., U.S. or other applicable export restrictions, including without limitation the U.S. International Traffic in Arms Regulations (ITAR) or special controls under the Export Administration Regulations (EAR), Customer will notify Mentor Graphics personnel, in advance of each instance of disclosure, that such information is subject to such export restrictions.

13. **U.S. GOVERNMENT LICENSE RIGHTS.** Software was developed entirely at private expense. The parties agree that all Software is commercial computer software within the meaning of the applicable acquisition regulations. Accordingly, pursuant to U.S. FAR 48 CFR 12.212 and DFAR 48 CFR 227.7202, use, duplication and disclosure of the Software by or for the U.S. government or a U.S. government subcontractor is subject solely to the terms and conditions set forth in this Agreement, which shall supersede any conflicting terms or conditions in any government order document, except for provisions which are contrary to applicable mandatory federal laws.

14. **THIRD PARTY BENEFICIARY.** Mentor Graphics Corporation, Mentor Graphics (Ireland) Limited, Microsoft Corporation and other licensors may be third party beneficiaries of this Agreement with the right to enforce the obligations set forth herein.

15. **REVIEW OF LICENSE USAGE.** Customer will monitor the access to and use of Software. With prior written notice and during Customer's normal business hours, Mentor Graphics may engage an internationally recognized accounting firm to review Customer's software monitoring system and records deemed relevant by the internationally recognized accounting firm to confirm Customer's compliance with the terms of this Agreement or U.S. or other local export laws. Such review may include FlexNet (or successor product) report log files that Customer shall capture and provide at Mentor Graphics' request. Customer shall make records available in electronic format and shall fully cooperate with data gathering to support the license review. Mentor Graphics shall bear the expense of any such review unless a material non-compliance is revealed. Mentor Graphics shall treat as confidential information all information gained as a result of any request or review and shall only use or disclose such information as required by law or to enforce its rights under this Agreement. The provisions of this Section 15 shall survive the termination of this Agreement.

16. **CONTROLLING LAW, JURISDICTION AND DISPUTE RESOLUTION.** The owners of certain Mentor Graphics intellectual property licensed under this Agreement are located in Ireland and the U.S. To promote consistency around the world, disputes shall be resolved as follows: excluding conflict of laws rules, this Agreement shall be governed by and construed under the laws of the State of Oregon, U.S., if Customer is located in North or South America, and the laws of Ireland if Customer is located outside of North or South America or Japan, and the laws of Japan if Customer is located in Japan. All disputes arising out of or in relation to this Agreement shall be submitted to the exclusive jurisdiction of the courts of Portland, Oregon when the laws of Oregon apply, or Dublin, Ireland when the laws of Ireland apply, or the Tokyo District Court when the laws of Japan apply. Notwithstanding the foregoing, all disputes in Asia (excluding Japan) arising out of or in relation to this Agreement shall be resolved by arbitration in Singapore before a single arbitrator to be appointed by the chairman of the Singapore International Arbitration Centre ("SIAC") to be conducted in the English language, in accordance with the Arbitration Rules of the SIAC in effect at the time of the dispute, which rules are deemed to be incorporated by reference in this section. Nothing in this section shall restrict Mentor Graphics' right to bring an action (including for example a motion for injunctive relief) against Customer in the jurisdiction where Customer's place of business is located. The United Nations Convention on Contracts for the International Sale of Goods does not apply to this Agreement.

17. **SEVERABILITY.** If any provision of this Agreement is held by a court of competent jurisdiction to be void, invalid, unenforceable or illegal, such provision shall be severed from this Agreement and the remaining provisions will remain in full force and effect.

18. **MISCELLANEOUS.** This Agreement contains the parties' entire understanding relating to its subject matter and supersedes all prior or contemporaneous agreements. Any translation of this Agreement is provided to comply with local legal requirements only. In the event of a dispute between the English and any non-English versions, the English version of this Agreement shall govern to the extent not prohibited by local law in the applicable jurisdiction. This Agreement may only be modified in writing, signed by an authorized representative of each party. Waiver of terms or excuse of breach must be in writing and shall not constitute subsequent consent, waiver or excuse.

Rev. 170330, Part No. 270941