Tutorial Overview

- Overview and basics
- Using the Tool Suite
- How to use sim-outorder
- How to build your own simulators
- How to modify the ISA
- How to use the memory extensions
- SimpleScalar limitations and caveats
- Wrapup

Limitations of the tools

- Important to understand for accurate research
    - Same simulator may be accurate in one study, not in another
    - Following is an incomplete list
- Simulator structure
- Processor model
- Memory system
- Simulation accuracy

Limitations of the simulator structure

- Functional core and timing simulator are split
  - Performance optimization
- Timing correctness difficult to ascertain (program runs)
- Some speculation (value pred.) inaccurate
- Multiprocessor target much harder to implement
  - Result of load may depend on timing
  - Functional core(s) has (have) no notion of time
  - Some memory models may work

Limitations of the processor model

- RUU model is one implementation
  - Reservation station and reorder buffer merged
  - Separate load-store queue
  - Different implementations may vary widely
- No partial forwards on LSQ
  - (example: byte read after word write)

Limitations of the memory system

- No causality in memory system
  - All events are calculated at time of first access
- No address translation
  - All addresses virtual
- Fixed latency TLB misses, no traffic
- No MSHRs in memory hierarchy
- Accurate if memory system is lightly utilized
  - Memory extensions address these limitations

Limitations of the simulation accuracy

- No system code modeled
  - Future releases may rectify this
- No validation against real system
  - Hard problem
- Simulator may be inaccurate depending on research!!!
- YOU are responsible for determining accuracy!